

Model Name: GA-P55A-UD3P 2.0

SHEET

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03	BLOCK DIAGRAM
04	CPU LGA1156-A
05	CPU LGA1156-B
06	CPU LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCH FDI,DMI,USB,PCIE,NVRAM
11	PCH DP,CLK BUFFER
12	PCH HOST,SATA,PCI
13	PCH GPIO,CTRL,AUDIO
14	PCH PWR,GND
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOT
18	PCI SLOT 1, 2, 3
19	ITE 8720 LPC IO
20	COM, -PROHOT , DYNAMIC OC , LPT
21	Dual BIOS
22	ALC889
23	REAR AUDIO JACK
24	CLOCK GEN ICS9LPRS914
25	VCORE PWM ISL6336CR-1
26	VCORE PWM ISL6336CR-2
27	CPU VTT PWM ISL6322G

28	DDR 15V & VCC1 05 PCH PWM ISL6545CBZ
29	DISCRETE POWER
30	F PANEL , F USB , FDD
31	ATX POWER
32	GSATA2-Marvell 9128
33	REALTEK RTL8111E
34	TPM SLB9635TT
35	HWM,KB/MS , FAN CTRL
36	ESATA JMB362
37	IT8213
38	UP720200
39	TABLE LIST
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GA-P55A-UD3P Version:2.0

Circuit or PCB layout change
for next version

Component value change history

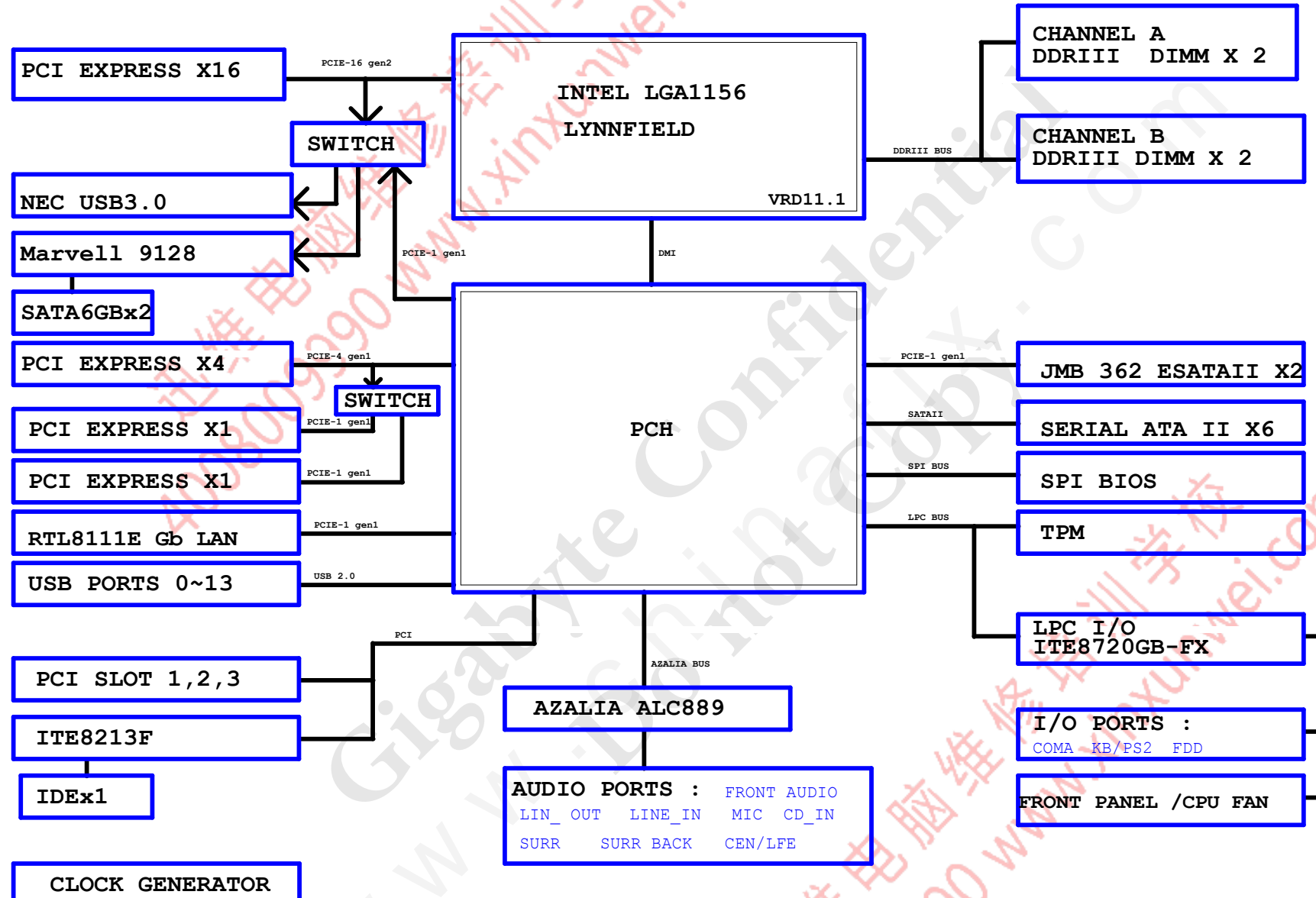
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EP55A-UD3P 0.2	1. CHECK +12V SHORT PAD FOR 10mil	9. L1U1,L1U4 RTL8111D --> RTL8111C
	2. F1_1394加蓋(包材階)	10. PCB "育富"移除
	3. ADD DR86=124K/4/1 , DR88=249K/4/1	11. ONFI指定用11SM1-600078-02R
	4. U12-U15 upi6262M --> upi6267M	12. R376 2.26K/4/1 --> 2.55K/4/1
	5. DRAM_PWROK R490=1K/4/1 , R491=3K/4/1	13. 確認上哪種upi6262 10%/upi6267?
	6. REMOVE DR138=0/4 , ADD DR139,DR141=0/4	14. FB7~FB10 REMOVE
	7. RU2指定料號:10HP4-112540-11R	15. PCH BUFFER 25MHz REMOVE "X2,C93,C94,R420"
	8. 排阻指定廠牌用WALSIN	16. BIOS 16M --> 32M (FOR ONFI ONBOARD)
2009/06/10 PBOM:0.1	1. NEW MODEL: P55-UD3P-0.1	
2009/06/24 EBOM:10A	1. ADD -RSMRST PATCH CIRCUIT R866~R868,C192,C193,Q112,Q113,3UDUAL_ICH ADD 5VSB R864,R865	
	2. CHANGE Marvel9123 gpio pin,del RR39,R10,RR67,RR65,ADD RR62	
	3. CHANGE IT8275 料號,DR84 100--->0	
	4. MARVELL 9123----->JMB363	
	5. J363/J632 PATCH POWER SEQUENCE;Q50 MOS--->BJT	
2009/07/7 PBOM:10B	1. P-BOM	
2009/07/10 PBOM:10C	1. RBC53 0.1UF----->1UF	
2009/07/16 PBOM:10D	1. 移除PLL電容,BC136,BC150,BC185,BC201	
2009/07/22 PBOM:10E	1. (CE2,EC32,EC37,EC38,EC23,EC36,REC3)100uf cap 6*6改成6.3*10.5mm,因缺料	
	2. VCC3_DAC直接由VCC3經0 ohm提供	
2009/07/29 PBOM:10F	1. ADD R190 1K/4/1 FOR PCIE OVERCLOCK	
2009/08/24 EBOM:29T	1. P55-UD3P-3.0 FOR 9123/USB3.0/8213	
2009/09/09 EBOM:29A	1. CHANGE 9123;USB3.0 MP料號	
	2. ADD SWITCH U29 FOR X16,GEN2 DEVICE分開用	
	3. 修正X4,X1SWITCH 線路	
2009/10/02 PBOM:10B	1. 修正CPU VCORE loadline阻值,choke料號,cpu socket料號,EUP	
2009/10/08 PBOM:10C	1. 修正NEC USB3.0 power sequence,UR6 8.2k--->47k,del UC54	
2009/11/03 PBOM:10D	1. DEL ESD3,ESD18,ESD19,BIOS ADD 30R替料	
2010/03/08 EBOM:20t	1. 8111C--->8111E 2..I PHONE 只保留前窗, NEC USB2.0直接接到後窗	
	3. GPIO21 改LO FOR MB_ID(R585),DEL R558	4. SATA FOOTPRINT 變更爲MASK
	5. ICS914及TPM 都換新版本	
2010/03/08 EBOM:20A	1. IRP2/IRP4 28K--->33K 2.r585 8.2k--->1k	
2010/04/15 PBOM:20B	1. IPB1 0.1UF----->1UF.ADD PACKAGE	2010/04/29 PBOM:20C 1. IPR1,IPR3 11.3K--->33K;IPR2,IPR4 33K--->11.3K

DATE	Change Item	Reason
EP55A-UD3P 0.2	1. REMOVE AUDIO ESD	7. 1394 "IEC1" NET SWAP & SHORT PROTECT
	2. REMOVE CPU_VAXG	8. PIN HEATER CHECK
	3. PCH_CLK 改 SHORT PAD (0 ohm維持10pcs以下)	9. ITE8275 SYS_RST PATCH
	4. ITE8275 GPIO11,GPIO13 TO TURBO0/TURBO1	10. BC118,BC119 --> TBC29,TBC30
	5. F_PANEL UPDATE H2X10PANEL-1	11. BC5靠近M_BIOS PIN8 , BC6靠近M_BIOS PIN8
	6. ONFI 改 ON BOARD	12. U2 7474 REMOVE
EP55-UD4P 0.2	1. ONFI作塞孔	
2009/05/20 PCB:0.1	1. NEW MODEL: P55-UD3P-0.1由EP55A-UD3P-0.2修改	
2009/06/10 PCB:0.1	1. NEW MODEL: P55-UD3LP-0.1由P55-UD3P-0.1修改	
2009/06/24 PCB:1.0	1. P55-UD3P-1.0 2. 修改文字面	
	3. ADD -RSMRST PATCH CIRCUIT,3UDUAL_ICH ADD 5VSB	
	4. ADD J362 POWER SEQUENCE PATCH CIRCUIT,VCC3&362_1.8V	
	5. MARVELL 9123--->J363 (SPEC 變動)	
2009/07/07 PCB:1.01	1. 修改文字面,加入crossFire X(PM-SALES REQUEST)	
	2. 連帶更改FB5.CR64,RN21 short-wire---->電阻;ESD17 5VDUAL--->5VSB	
2009/08/21 PCB:2.9T	1. P55-UD3P-3.0 FOR 9123/USB3.0	
	2. 實驗4層板及6層板(不同內層切割)	
2009/09/08 PCB:2.91	1. ADD PCIEX1 SLOT DETECT PIN FOR BIOS	
	2. EACH USB PORT USE ONE POLYFUSE	
	3. 修正X16/X8 TURBO MODE 線路	
	4. 調整PCICLK,USB_SEL GPIO GP40 TO GP23	
2009/10/02 PCB:1.01	1. 由 REV:2.91改爲REV:1.01 FOR MP	
2010/03/05 PCB:2.0T	1. R879 改接3VDUAL FOR NCT3931預留	5. NEC USB3.0 ADD UR12 預留FOR POWER SEQUENCE
	2. F_USB1增加iPhone charge circuit	6. TPM ADD TR23 FOR 3VDUAL_ICH
	3. CR53 DOWN SIZE	7. I PHONE 只保留前窗, NEC USB2.0直接接到後窗
	4. SR2,SR3,SR4,SR5 footprint改爲mask	8. USB3_TURBO,9128_TURBO GPIO PIN改接至PCH
	9. 8111C--->8111E	
2010/03/30 PCB:2.0	1. Add IPR14,IPBC2,IPCD1	
	2. Remove EC34	

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BLOCK DIAGRAM

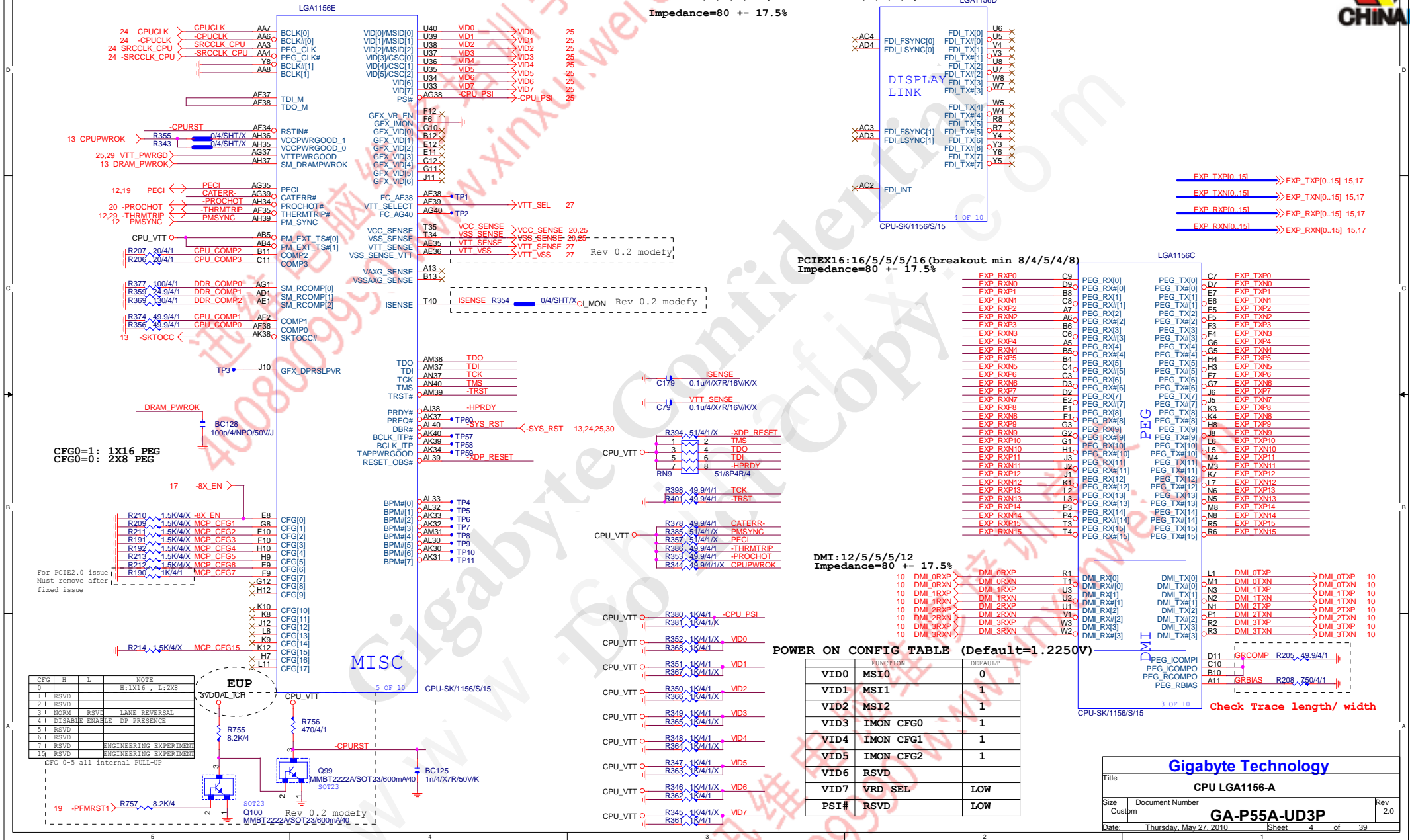


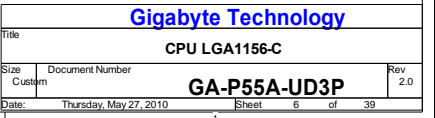
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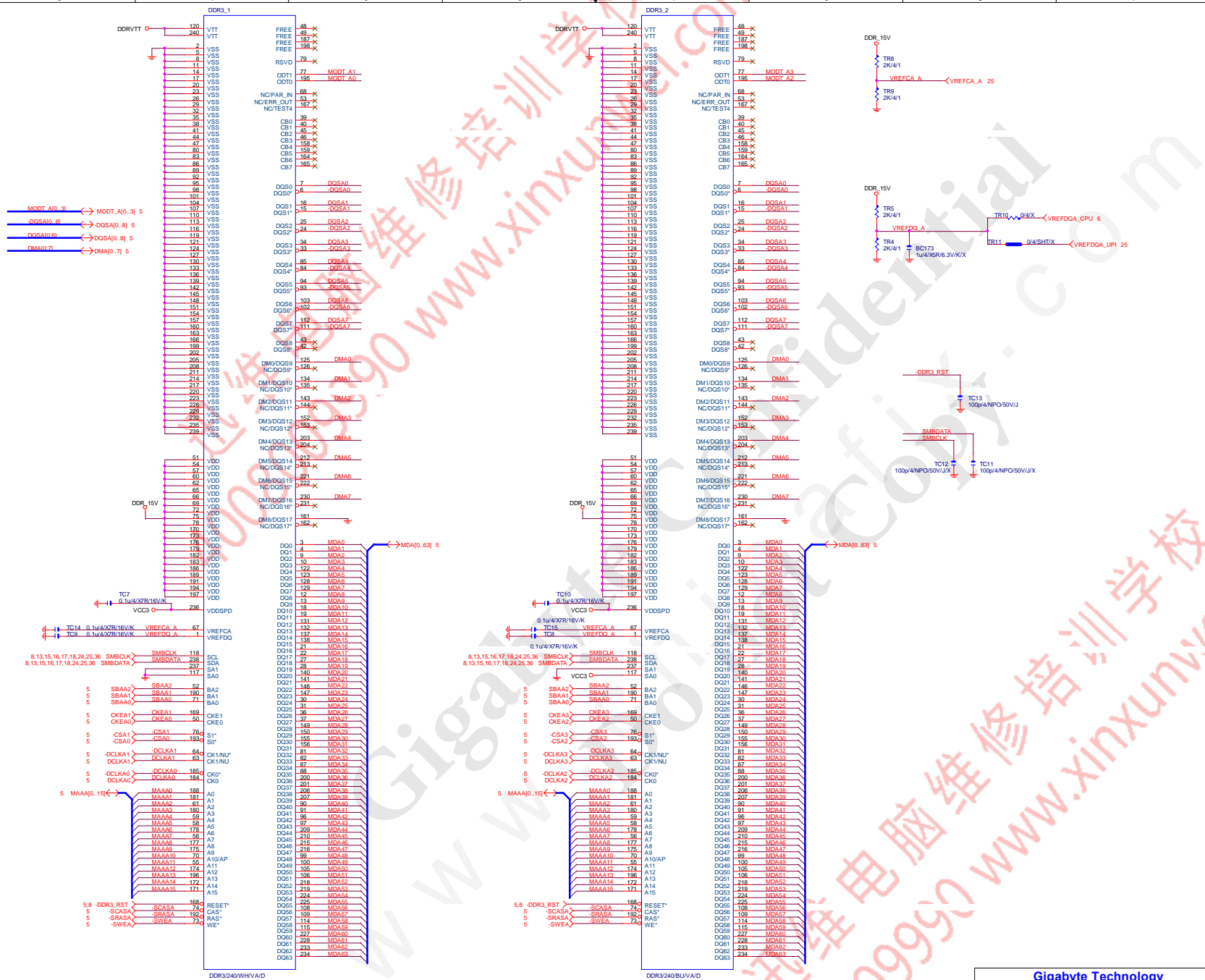
FDI : 16/5/5/16(breakout min 8/4/5/4/8)

Impedance=80 +- 17.5%

LGA1156D







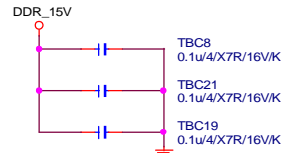
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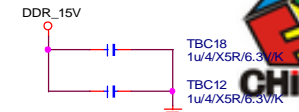
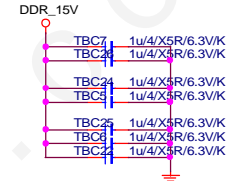
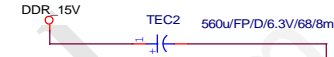
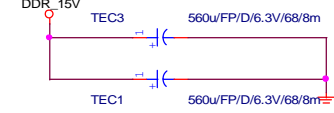
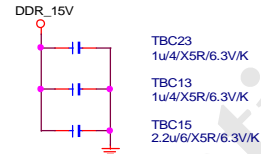
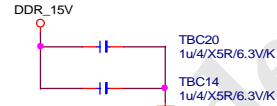
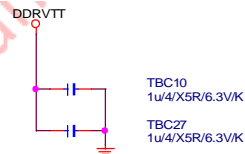
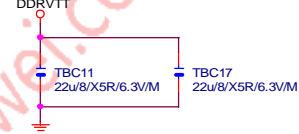
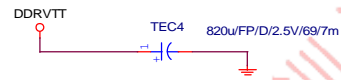
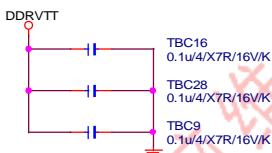


DDR TERMINATION CHANNEL A/B

DDR15V Decouple



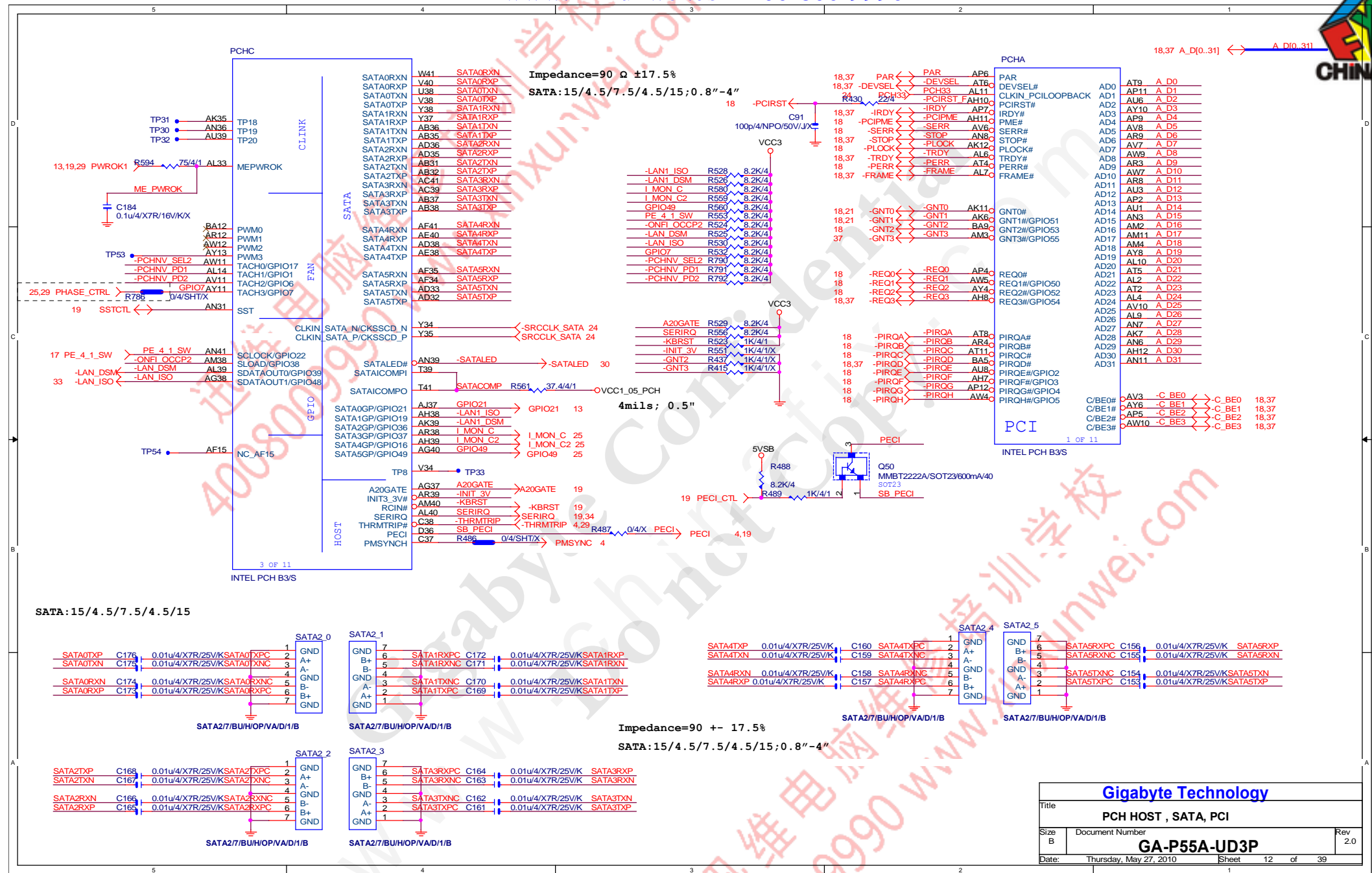
DDRVTT Decouple



COUPON1 COUPON1 1 2 COUPONX VCORE

COUPON2 COUPON2 1 2 COUPONX

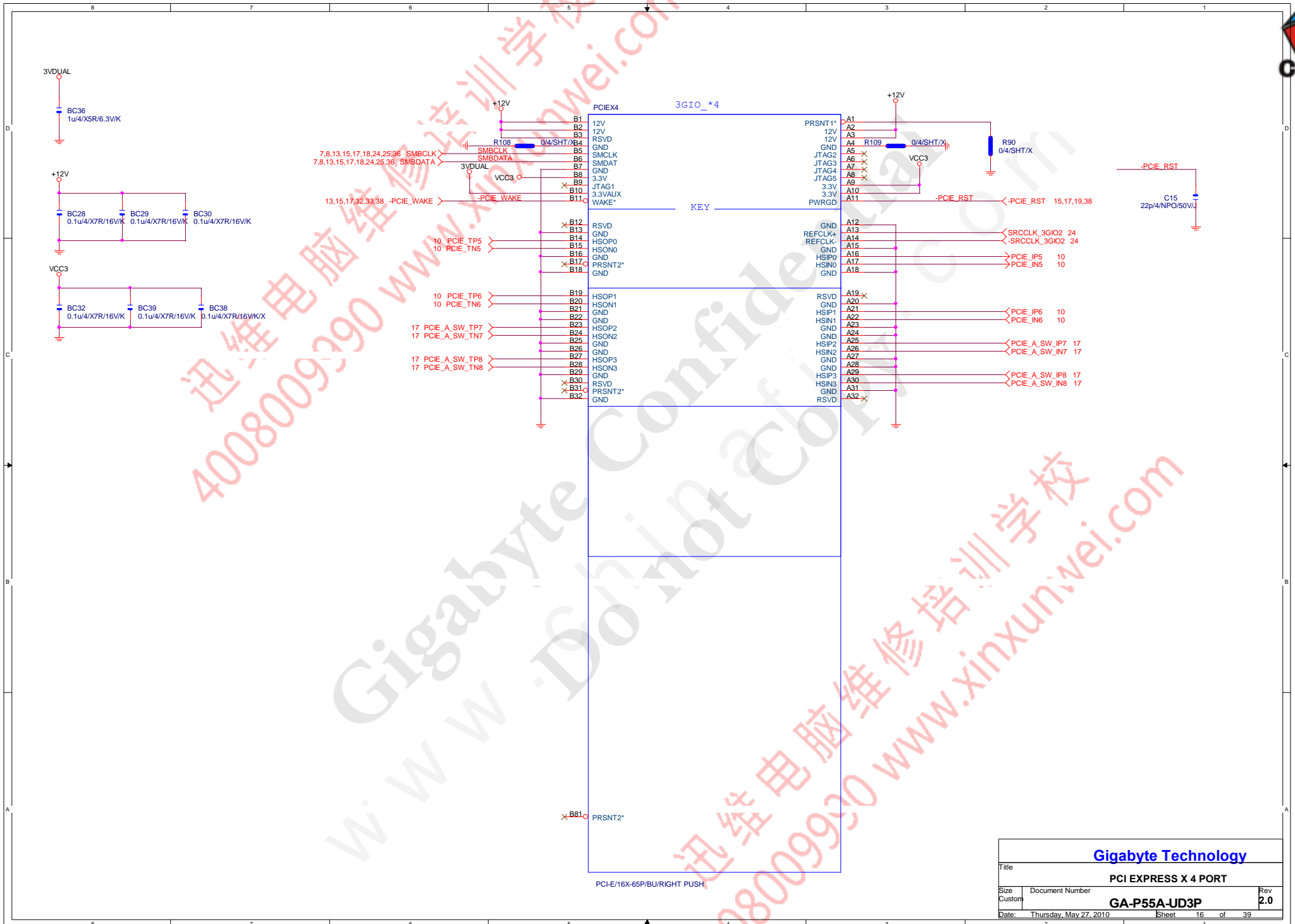
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DDRIII POWER CAP			
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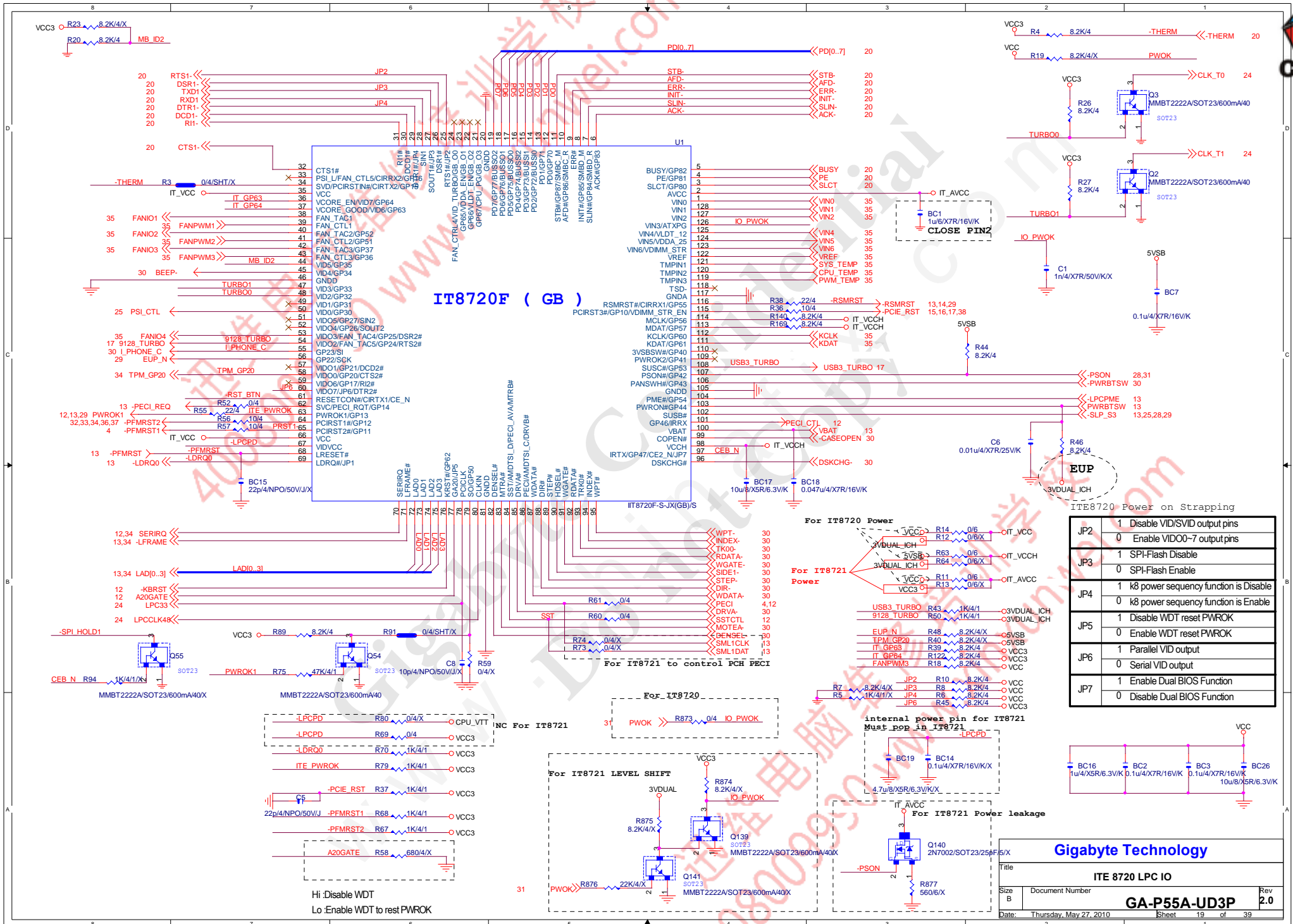




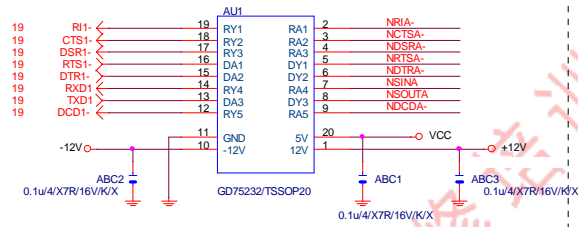
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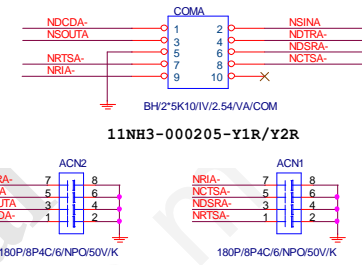
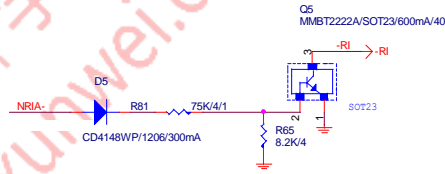




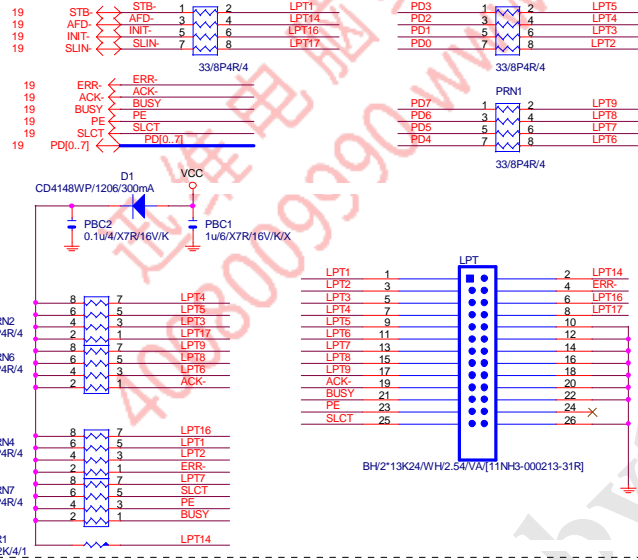
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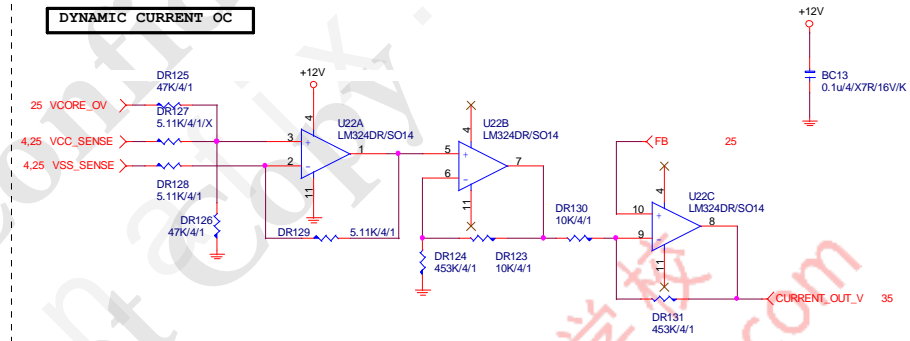
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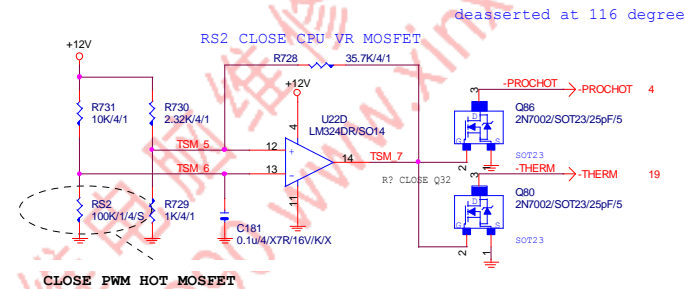
LPT PORT



DYNAMIC CURRENT OC



-PROHOT



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VCC3
BC215
0.1u/4/X7R/16V/K

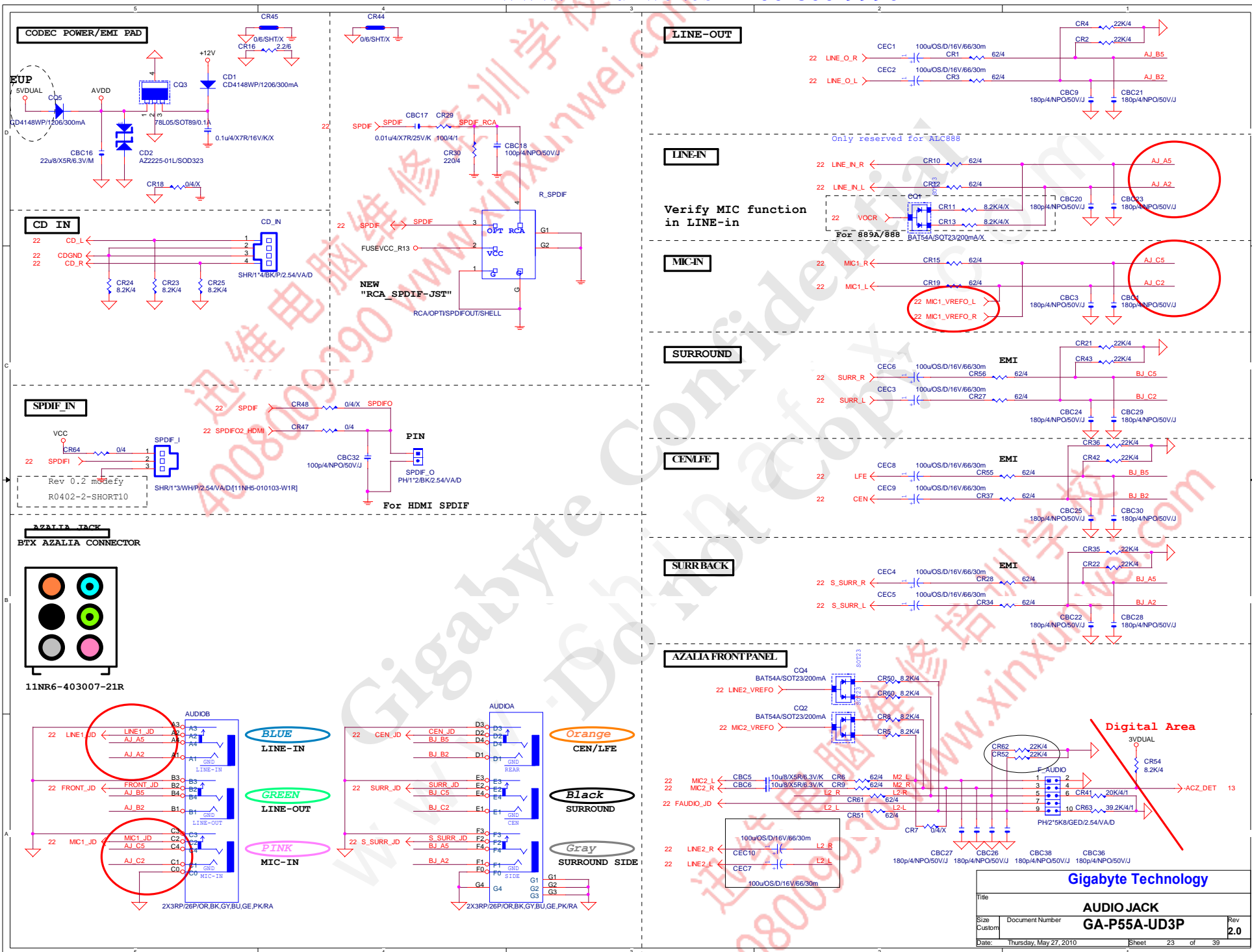
r1.0 DG;0.7 CRB

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

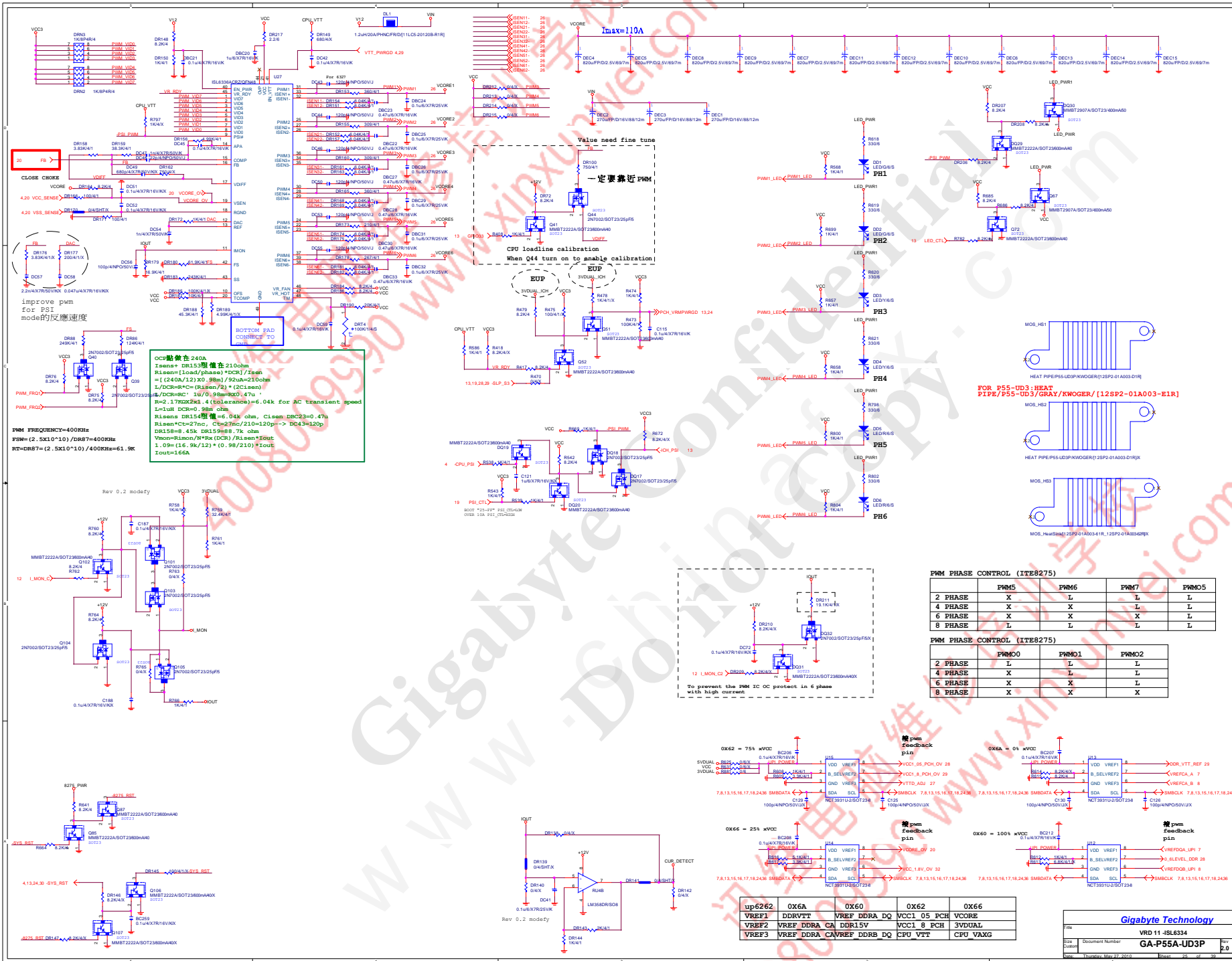
1 means floating
0 means PD 1K

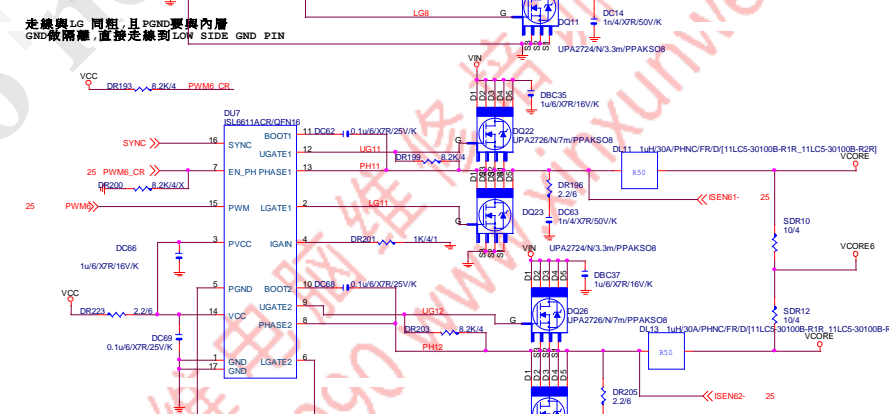
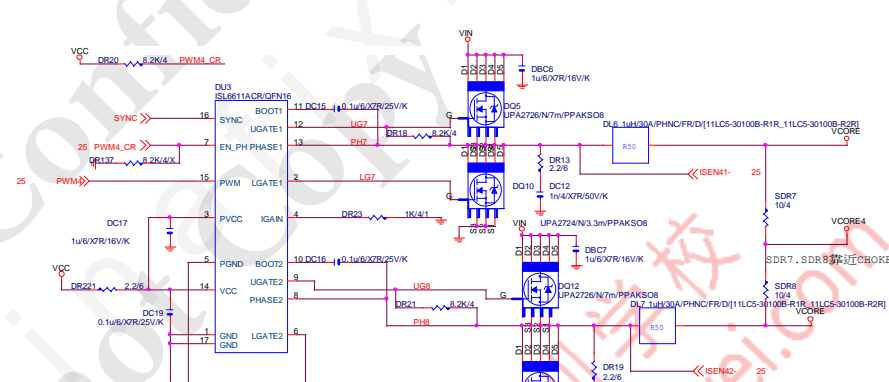
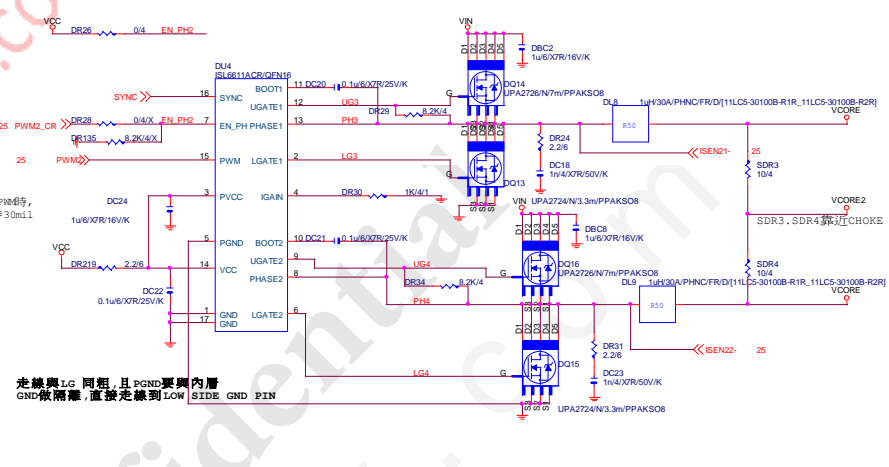
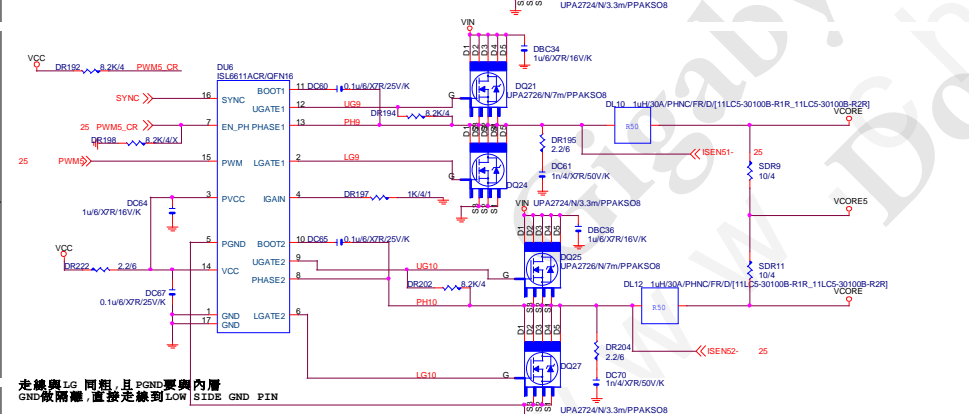
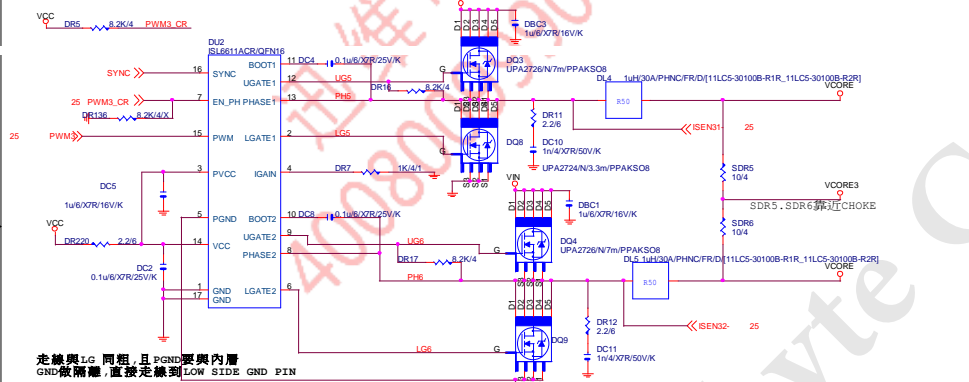
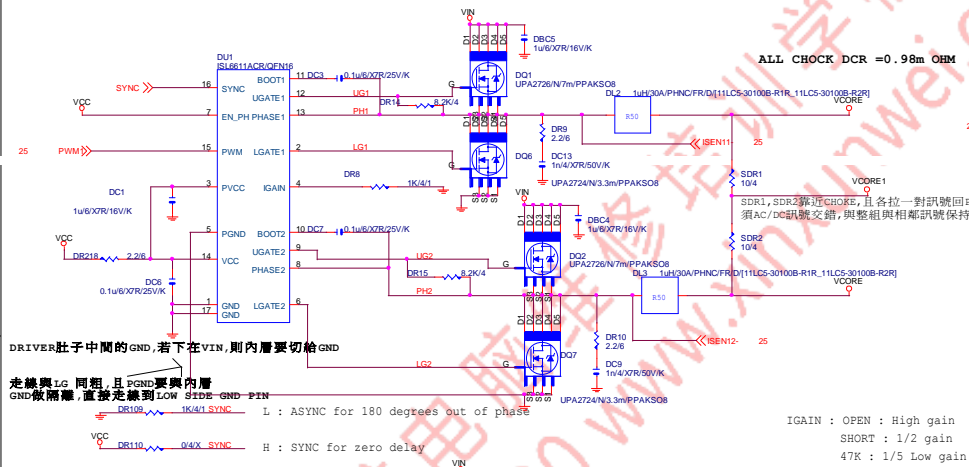
IC8SO-SOCKET

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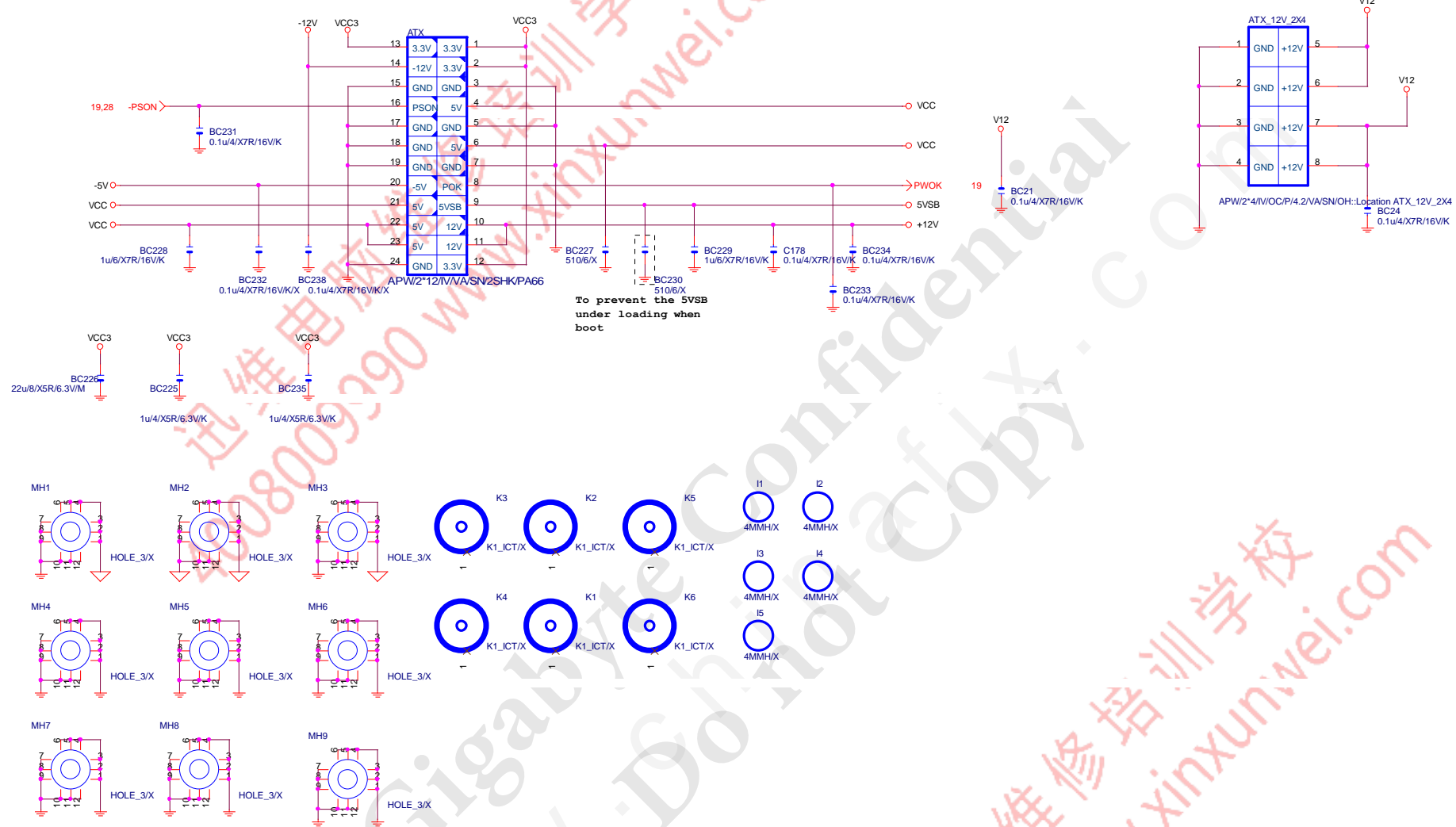




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ATX POWER CONNECTOR



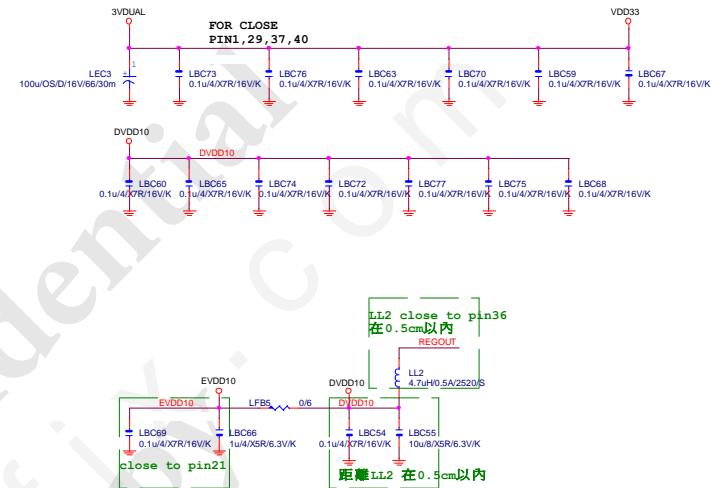
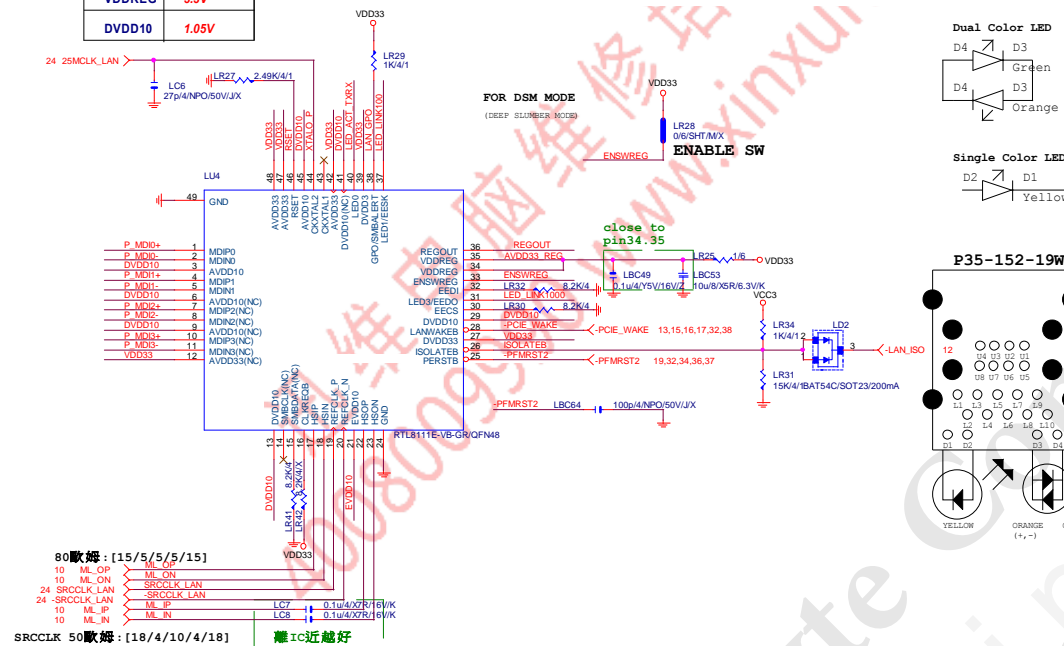
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ATX POWER CONNECTOR		
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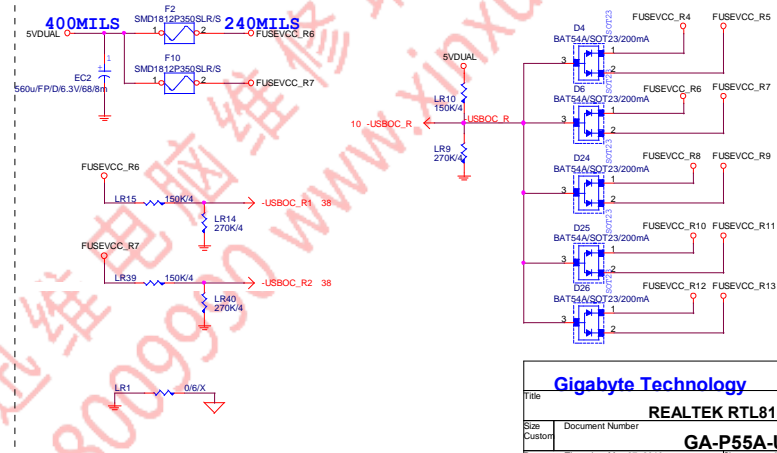
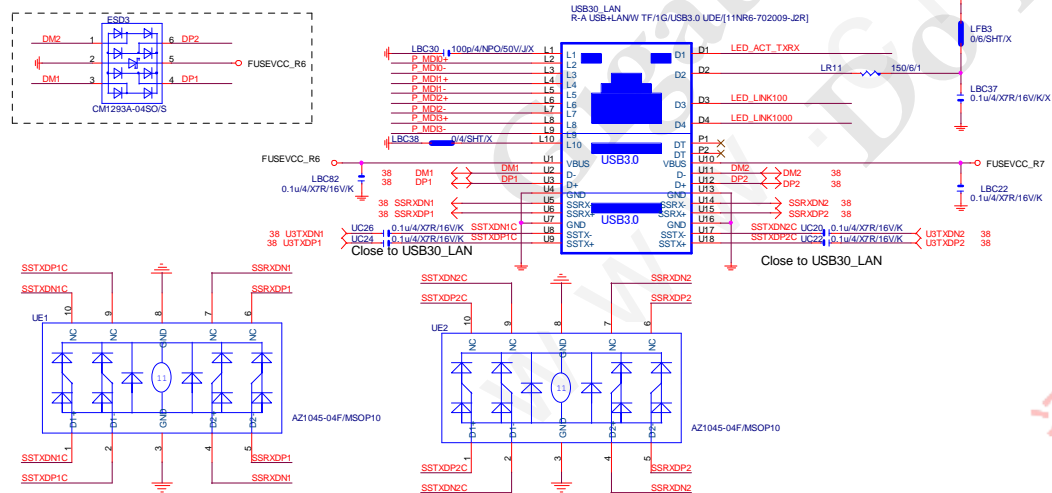
PCIE-1G LAN

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB30 LAN CONNECTOR



SEL	OE	Y+	Y-
X	H	H1-Z	H1-Z
L	L	M+	M-
R	R	D+	D-

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